Physics and Compact Modeling of SOI Substrates with Buried Ground Plane (GPSOI) for Substrate Noise Suppression

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***Abstract* — The physical mechanisms responsible for superior cross-talk suppression are identified in a new class of silicon-on-insulator substrate (GPSOI) that incorporates a buried metallic ground plane below the active silicon and buried oxide layers. It has been shown [1] that this technology exhibits a factor of ten reduction in cross-talk power between components through the substrate compared to existing state-of-the-art silicon-based substrates using standard s_{21} magnitude measurements in a microwave coplanar transmission test structure. The dominant cross-talk mechanisms are identified and compared to other existing cross-talk suppression technologies using numerical electro-magnetic simulations and lumped element compact model development.**

I. Introduction

Substrate crosstalk presents fundamental limitations to the realization of mixed signal RF/microwave IC's. The performance of RF analog circuits in integrated mixed signal telecommunication IC's can be compromised by cross-talk through the substrate from adjacent digital circuits. This problem becomes more severe as the frequency increases, particularly for silicon-on-insulator substrates where the buried oxide becomes transparent to high frequency a.c. and transient signals [2]. Substrate crosstalk can be reduced by manufacturing a substrate with inherent crosstalk suppression capabilities including the use of high resistivity substrates (i.e. 200 Ω-cm resistivity) [2], [6]. Structures such as guard rings and dielectric trenches can also be utilized alone or in combination with high resistivity substrates. At the present time, the greatest substrate noise suppression has been obtained [2] using high resistivity SOI substrates with diffused guard rings.

In this paper a new substrate called Ground Plane Silicon-On-Insulator (GPSOI) is presented and is shown to offer 20 dB increased crosstalk suppression compared to high resistivity SOI substrates that use guard rings [2]. The GPSOI is a SOI substrate incorporating a buried metallic layer below the active silicon and buried oxide layers. This metallic plane may be connected to ground forming a ground plane.

The following sections describe the ground plane substrate and the fabricated crosstalk test structures for this work. The experimental measurement data presented in [1] are explained with the aid of numerical electromagnetic simulations. An equivalent lumped element model is also presented and its performance is evaluated against measurements and numerical simulation results.

II. Crosstalk Test Structures In The GPSOI Substrate

As depicted in Fig. 1, the buried metallic plane of GPSOI substrates located below the buried oxide layer at the oxide-silicon interface is a layer of WSi_2 0.2 μm thick with a resistivity of 40 μΩ-cm. The silicon substrate is n-type with a resistivity of 9-15 Ω-cm and the buried CVD oxide is 1.0 μm thick. Such a substrate is manufactured by a silicon bonding technology similar to silicon-on-silicide or metal-on-insulator (SSI or SMI) substrates [3]. The fabrication of GPSOI substrates for this work took place in the Department of Electrical and Computer Engineering of the Queen's University of Belfast, UK. Further details of the GPSOI manufacturing process will not be mentioned as they are beyond the scope of this paper.

For the purpose of this study, substrate crosstalk test structures have been designed and fabricated on GPSOI substrates. To make comparisons to the work of [2] meaningful, and to isolate only the cross-talk mechanisms associated with the substrate itself, the silicon active layer above the buried oxide was not present in these experiments. Cross-talk through the silicon active layer of an SOI wafer can be suppressed using conventional techniques such as trenches and diffusions between sensitive elements.

Three substrate configurations were considered. The first one involved connecting the buried WSi_2 layer to the

surface ground by means of top down contacts. This substrate configuration will be referred to as locally grounded GPSOI substrate. Fig. 1 depicts a test structure for the grounded GPSOI experiments. To make comparisons to the work of [2] meaningful, the same size of Al square pads (50 μm x 50 μm) where used as transmitter (Tx) and receiver (Rx) for the s21 transmission measurements. The separation distance between the transmitter/receiver (Tx/Rx) pads was varied to be 75, 100, 150 and 200 μm. The two pads were embedded in a coplanar wave-guide (CPW) ground-signal-ground (GSG) structure.

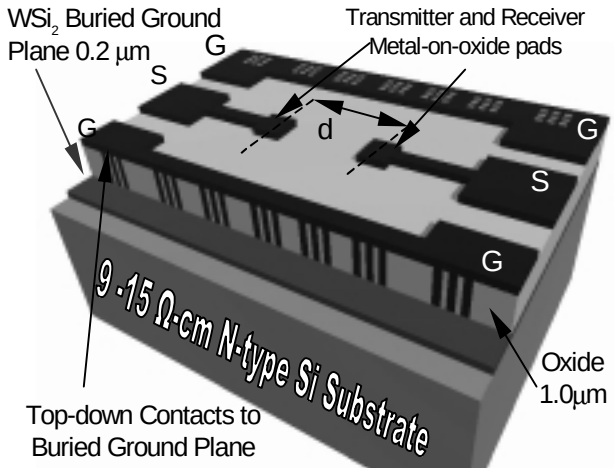

Fig. 1. The CPW crosstalk test structure with a grounded buried ground plane (Grounded GPSOI).

The case of an electrically floating buried ground plane was investigated by a second substrate configuration, which will be referred to as the floating GPSOI, where the top-down contacts were absent. The final configuration involved a substrate without a buried ground plane that represented conventional SOI technology. The oxide thickness for the latter configuration was 1.2 μm, equivalent to the thicknesses of the top CVD oxide and the WSi_2 plane combined. This configuration will also be referred to as the control or standard (15 Ω-cm) resistivity SOI in later sections, in contrast to high resistivity SOI substrates that have 200 Ω-cm substrate resistivity.

The s-parameters of the two-port test structures were measured using an HP 8510C on-wafer s-parameter 50 Ω characteristic impedance characterization system in the frequency range of 500 MHz to 50 GHz with tungsten-tip 150 μm pitch Cascade air-coplanar probes. The magnitude of the forward transmission scattering parameter s_{21} versus frequency provides a quantitative measure of the degree of isolation between the transmitter and receiver and a figure of performance that facilitates comparison with published data [2], [4].

Fig. 2 shows s_{21} vs. frequency plots of standard (20 Ω-cm) and high resistivity (200 Ω-cm) SOI substrates as measured by [2] and how they compare with this work. The measurements shown have been performed on a test structure with 100 μm separation between the Tx/Rx pads in the range of 500 MHz and 50 GHz. Data [2] from measurements of test structures with diffused guard rings and diffused Tx/Rx pads are also shown for comparison. The guard ring structures have shallow diffusions as Tx/Rx pads, which result in an effective oxide thickness of 0.4 μm. The locally grounded GPSOI structures have exhibited the highest degree of isolation compared to all other SOI structures. The degree of isolation ranged from 90 dB at 500 MHz to 50 dB at 50 GHz. The control provided less that 40 dB of isolation at 500 MHz rising to less than 30 dB at the end of the frequency range. It can be observed from Fig. 2 that a very good agreement between the two control SOI structures (i.e. that of this work and that of [2]) has been achieved for the same separation distance.

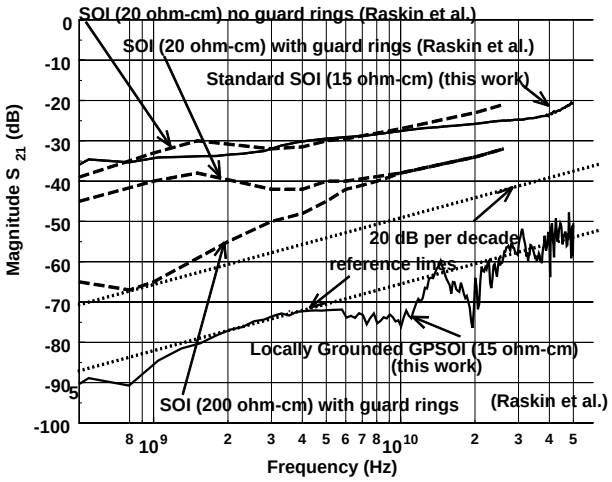

Fig. 2. Measurements of the magnitude of the s_{21} transmission parameter for the locally grounded cross-talk structure on GPSOI and the standard SOI. Results from previous work on low and high resistivity substrate SOI with and without guard rings [2] are shown for comparison. Pad separation was d=100 μm and Tx/Rx pad areas were 50 μm × 50 μm for all cases.

III. Simulations And Measurements

The s_{21} transmission magnitude was simulated for the entire test structure shown in Fig. 1 including probe pads using numerical multidimensional electro-magnetic modeling in Momentum, a quasi-3D simulator that is part of the HP Advanced Design System (HPADS) software suite [5].

Comparisons between simulations and measurements for all three substrate configurations are shown in Fig. 3, where the separation distance between Tx and Rx pads was 100 microns. Excellent agreement is obtained between simulated and measured results up to 10 GHz for the locally grounded GPSOI, and over the entire measured frequency range for the floating GPSOI and control SOI structures. From the detailed modeling to be discussed in the next section, deviations between simulations and measurements above 10 GHz for the grounded GPSOI can be attributed to cross-talk between the probes themselves through the air above the substrate which was not accounted for in the simulations. Below 10 GHz, where the probe cross-talk does not dominate, the s_{21} transmission exhibits a 20 dB per decade increase with frequency indicating that there is a single RC time constant responsible for cross-talk between the Tx/Rx pads in the grounded GPSOI. For the floating GPSOI structure, cross-talk increases dramatically compared to the locally grounded GPSOI. A similar effect of a floating conductive plane has been discussed by [2] in the form of a floating heavily doped buried layer. Its low resistivity helps the spreading of noise to other parts of the chip rather than shunting it to ground, as the electrically floating high conductivity layer simply acts as a common fluctuating iso-potential node beneath all circuit components.

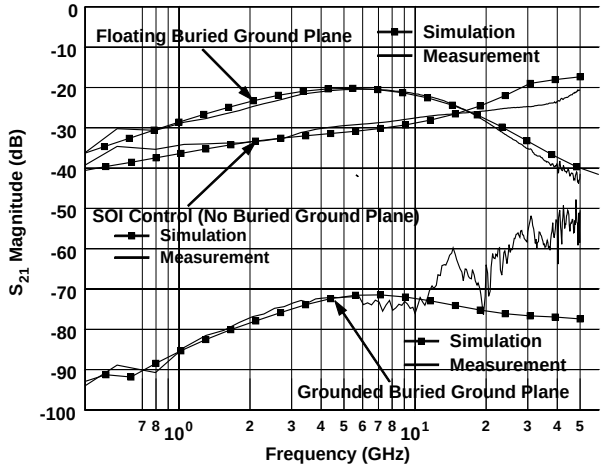

Fig. 3. Comparison of measurement and numerical electro-magnetic simulation results for the locally grounded GPSOI, electrically floating GPSOI, and the control SOI. Separation distance is 100 μm between Tx and Rx pads.

Both the numerical simulations and measurements of s_{21} for the grounded GPSOI revealed that s_{21} cross-talk decreased by approximately 2 dB per 50 micron increased spacing between Tx/Rx probes over the entire frequency range, with the exception of the measurement results above 10 GHz where it appears that the cross-talk between the probes themselves was dominating.

IV. Equivalent Lumped Element Model

A lumped equivalent circuit model, shown in Fig. 4, can be used to explain the physical mechanisms responsible for cross-talk in the grounded GPSOI, as well as to explain the differences in cross-talk in comparison to SOI with no buried ground plane. For the grounded GPSOI structure, the elements C_1, C_2, $C_{PROBE\ PAD}$, R_1, and R_2 give rise to the observed s_{21} cross-talk measurements in the grounded GPSOI. The resistances R_1 and R_2 represent the finite resistance of the ground plane between the Tx/Rx pads, and between these pads and ground, respectively.

For SOI without ground planes, all elements are required expect R_1, and R_2. The local grounding for the grounded GPSOI shunts out the substrate elements C_3, C_{SI}, R_3, and R_{SI}, which model the substrate itself. C_2 accounts for capacitance between the Tx/Rx pads through the air and through the buried oxide regions, and C_3 accounts for capacitance between the Tx/Rx pads through the silicon substrate itself.

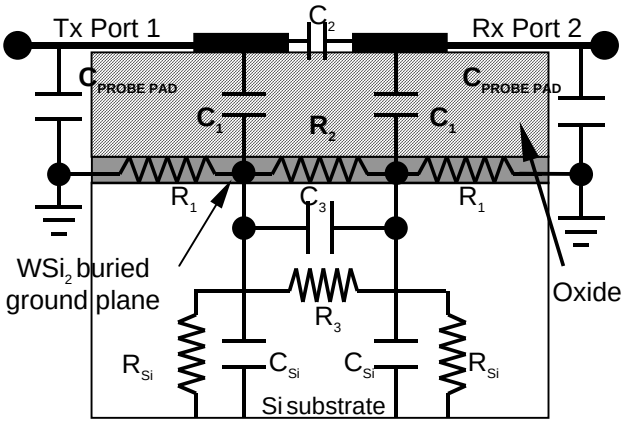

Fig. 4. Lumped element model.

The essential physical difference between the grounded GPSOI and the SOI structures without ground planes is the fact that the capacitance C_3 is eliminated in the grounded GPSOI thereby eliminating the impact of the much higher dielectric constant region of the silicon substrate and therefore providing significantly improved cross-talk isolation compared to SOI without ground planes. Model parameter extraction using a combination of geometrical considerations and parameter optimization reveal that C_2 is 93 aF for the grounded GPSOI with 100 micron spacing between the Tx/Rx pads. Detailed modeling of the SOI structure of [2] without ground planes and with guard rings and a high (200 Ω-cm)

resistivity substrate reveal that C_3 is approximately 30 times larger than C_2 for the same Tx/Rx spacing. This increase in cross-talk capacitance is due partly to the increased dielectric constant of the silicon substrate by a factor of three compared to the buried oxide. Additional observed increases in cross-talk in the SOI without ground planes are due to the fact that the area of C_3 is effectively much larger than that of C_2 due to the three dimensional nature of the structures.

Fig. 5 shows comparisons between measurements, numerical simulations, and lumped element modeling of the grounded GPSOI substrate for 100 micron spacing between Tx/Rx pads. The impact of the probe pad capacitances $C_{PROBE\ PAD}$ on s_{21} transmission has been determined using the lumped element model of Fig. 5 with and without the inclusion of the $C_{PROBE-\ PAD}$ capacitances. The probe pads will shunt energy to ground at high frequencies through the dielectric if the substrate has a ground reference thereby reducing the observed s_{21} crosstalk. From Fig. 5 it can be seen that both the numerical simulations and the lumped model with $C_{PROBE-PAD}$ included show that s_{21} peaks at a frequency which can be predicted from $f_1 = 1 / [\ 2\ \pi\ Z_o\ (C_1 + C_{PROBE-PAD})]$, where Z_o is the 50 Ω characteristic impedance of the source and load to the probes.

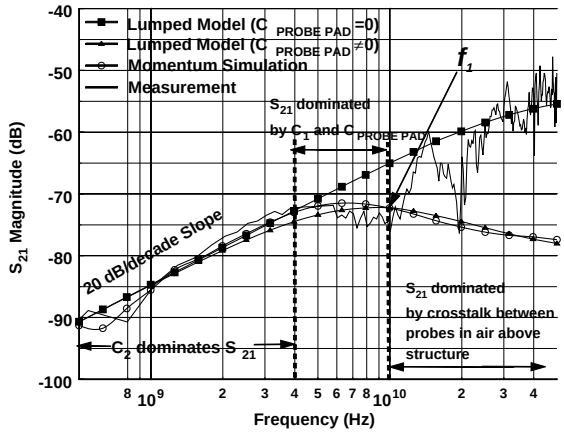

Fig. 5. Comparison of grounded GPSOI measurements, numerical simulations, and lumped models for a Tx/Rx pad separation of 100 μm.

Eliminating the effect of $C_{PROBE\ PAD,}$ as shown in Fig. 5, reveals that the cross-talk between the Tx/Rx pads is dominated the cross-talk capacitance C_2 up to nearly 50 GHz until C_1, which is much smaller than $C_{PROBE\ PAD}$, begins to shunt energy to the ground plane reducing the 20 dB per decade increase in s_{21} that occurs at the lower frequencies. Fig. 5 also shows the different frequency ranges where the various lumped element model components dominate.

V. Conclusions

Through detailed electro-magnetic modeling and compact model development, the physical mechanisms were identified which are responsible for the superior cross talk capability demonstrated by the GPSOI substrate technology compared to other reported substrates designed for substrate noise suppression. In summary, the cross talk capacitance is greatly reduced in the locally grounded GPSOI substrates compared to SOI substrates with no buried ground planes. The reduced cross talk capacitance arises in the grounded GPSOI due to the termination of electric field lines at the ground plane preventing penetration into the higher dielectric constant silicon substrate in contrast to SOI substrates with no ground planes. This results in a factor of ten improvement in cross talk suppression in the GPSOI substrates that possess a standard substrate resistivity (e.g. 15 Ω-cm) compared to state-of-the-art SOI technology using high resistivity substrates and guard rings.

Lumped element modeling enables the impact of the cross talk test structure probe pads to be taken into account in the presence of a grounded ground plane. The new lumped element model that was developed for the GPSOI substrate will prove useful in evaluating the substrate as a cross talk suppression strategy for mixed signal telecommunication circuits using SPICE level circuit simulation.

References

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